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Low Power Asynchronous Viterbi Decoder Using Hybrid Register Exchange Method

Mr. Girish D. Korde[1], Dr. Sanjay L. Haridas[2]
[1]*B. D. College of Engg., Sevagram, Wardha (M.S.),*
[2]*G. H. Raisoni Academy of Engg. & Technology, Nagpur (M.S.),*
Corresponding Author: Mr. Girish D. Korde[1]

***Abstract*:** *Viterbi decoders are widely used in digital communication which dissipates huge quantity of power. High speed and low power of system can be achieved by applying asynchronous technique to the digital system. In this work we have designed VD with 4-state, 1/2-code rate synchronous and asynchronous Viterbi decoder. Dynamic power can be lower by reducing switching activity and this is occurring due to designing VD from Hybrid Register Exchange Method. Soft decision decoding technique is being used since it can correct more number of errors than hard decision. Results shows that the implemented design using GALS gives 13.04% reduction in dynamic power consumption compared with its synchronous counterpart with improvement in maximum frequency by 52.71%.*

Keywords- *Viterbi Algorithm (VA), Viterbi decoder (VD), Branch Metric Unit (BMU), Add-Compare- Select (ACS), State Metric Unit (SMU), Hybrid Register Exchange Method (HREM).*

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I. Introduction

Viterbi is firstly introduces by Andrew J. Viterbi [1] in 1967, considering the VA is efficient method for decoding convolutional code. The objective of this work is to explore the design of a Viterbi decoder for wireless applications. Synchronous and Asynchronous are the two design styles existing for the realization of digital communication systems. Synchronous systems work with global clock and so has higher switching activity than asynchronous system. As switching activity is more in case of synchronous system power consumption is higher. Asynchronous systems are controlled by local clock or by dividing global clock resulting low switching activity. Since switching activity is low, speed of the system increases at the same time power consumption is reduced. Numerous advantages can be obtain from asynchronous designs with the use of a global clock. Switching activity is related only when system performing useful work. This is the important trait for battery operated systems. Worst case path delay can be used to determine the speed of synchronous systems which determines the maximum clock frequency. Asynchronous systems run on the average path delay of all their components [1]. With the increasing demand of wireless multimedia business, it is necessary to call for strict criterion on speed & power consumption of portable devices. With increasing of the transistor count & difficulty to propagate clock signals through an entire circuit VLSI designer suffers big problem. To tackle such a problem designers resort more & more to Globally Asynchronous Locally Synchronous (GALS)[1,2] or totally asynchronous solutions. Asynchronous circuits can be design using two different methods. First is bundle data (BD)[2] which relies on delay lines. Second approach is delay insensitive (DI)[2] relies on dual rail scheme, can be categories into several subcategories as pure delay insensitive (DI), Quasi Delay Insensitive (QDI)[2] and Speed independent circuits (SI) [2]. To reduce area & switching activity bundle data approach uses handshaking, but it faces technology related problem. Extra care with the computation of timing constraints between data & control signals is required [2]. QDI approach can be classified into several templates according to design technique. This yield high performance circuits but they are much larger than their synchronous counterparts. One of the most adopted templates is Delay-Insensitive Min-term Synthesis (DIMS) [2] for implementing QDI logic but it requires more space and logic elements with correspondingly high cost. Hard decision and soft decision are the two decoding techniques can be use for design of Viterbi decoder. Hard decision technique can identify any number of errors which are less than or equal to the correction capacity of the code. Soft decision technique decodes correctly any corrupted sequence with one or two errors independently of the quantification levels attributed to the symbols of a given received sequence. [3] This paper is divided into several sections as; Section 2 gives a brief description about convolution encoder and the Viterbi algorithm (VA). Section 3 details the proposed asynchronous Viterbi decoder followed by hybrid register exchange method (HREM) in section 4. Section 5 is devoted to the Results & discussion. A conclusion will found in section 6 followed by references.

II. Viterbi Algorithm

A brief description about Viterbi decoder is given in this section used to decode data encoded using convolutional encoder.

2.1 Convolutional encoder

To encode the input data we use convolutional encoder (k, n, K), where k number of output bits, n is number of input bits, and a constraint length K. There are 2^{K-1} states in VD. Therefore, there are 2^{K-1} surviving paths at each stage, and 2^K -1 metrics, one for each surviving path. For the formal specification, here we use (2, 1, 3) convolutional code. Thus, we can defined that the number of states in the trellis is 4. The generator polynomial for the encoder is given by: g1 = [1, 1, 1] and g2 = [1, 0, 1]. So two memory elements will be require for designing convolution encoder for code rate ½ and constraint length 3. Encoder design will work in serially time shifted data sequence manner. It involves the modulo-2 addition to generate output of selected input bit. Convolution encoder can easily represented by state diagram, tree diagram & trellis diagram [4].

2.2 Trellis Diagram

A message encoded using a convolution encoder follows called a trellis diagram. Each state transition on the diagram corresponds to a pair of output bits. There are only two allowed transitions for every state, so there are two allowed pairs of output bits, and the two other pairs are forbidden. If an error occurs, it is very likely that the receiver will get a set of forbidden pairs, which don't constitute a path on the trellis diagram. So, the task of the decoder is to find a path on the trellis diagram which is the closest match to the received sequence.

2.3 Viterbi Decoding Algorithm [1]

The Viterbi decoder is assumed to be integrated in a larger synchronous system using a serial to parallel interface which continuously receives 2-bit symbols. Two bit output is generated for one input bit is first converted into soft decision. To implement a soft-decision VD, the output of the encoder is translated from (0, 1) to (101, 011). 101 is the two's complement representation of the decimal number -3, and 011 is the representation of the decimal number 3 and then passes them to the Branch Metric Unit (BMU). The BMU computes the branch metric of each branch of the trellis by using Hamming distance. Each branch metric is added to the corresponding state metric, in the State Metric Unit (SMU), to generate the new state metric. The Add-Compare-Select unit receives two branch metrics and the state metrics. An ACS module adds each incoming branch metric of the state to the corresponding state metric and compares the two results to select a smaller one. The survivor path unit records the survivor path of each state selected by the ACS module. Once the trellis diagram is reconstructed, tracing back through the trellis is performed.

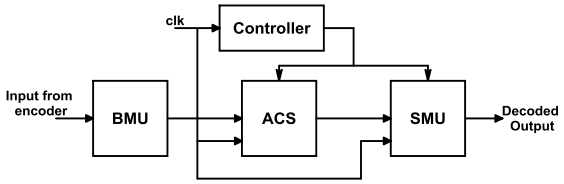

Figure 1: Synchronous Viterbi Decoder Using HREM.

In the Viterbi decoder; the register-exchange method is used to finish the survivor path storage and decoding. Frequent switching is the main disadvantage of register exchange method and long constraint length. The new proposed method designed for decoding data bits is known as hybrid register exchange method (HREM) [5]. Using this method switching activity can be reduced. Initial state can be first traced through an m cycle, and then transfer the content of initial state to the current state and the next m bits of the register is the m bits of current state itself.

III. Proposed Viterbi Decoder

Figure 2 shows the design of GALS Viterbi decoder. It consists of BMU, ACS, and SMU and controller which synchronize all blocks of VD asynchronously. Output of the encoder is given to the BMU. ACSU unit plays vital role. Here BM adds to the corresponding PM & generates new PM. New PM is compared with old PM & then store in PMM. ACSU store associated survivor path decision in the SMU. Controller unit consist of pointer which helps to keep the track of data exchange in SMU. It consists of one three bit counter unit and completion detection unit which helps in handshaking. Four phase handshaking is used to synchronize data between ACS and SMU block.

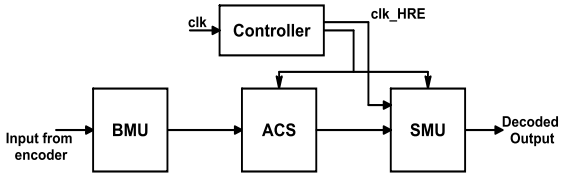

Figure 2: Proposed Asynchronous Viterbi Decoder Using HREM.

From the Figure 3, associated with each trellis state S at time t is a path metric $PM_t(p)$ and $PM_t(q)$ which is the accumulated metric along the shortest path leading to that state. The path metrics at time t can be recursively calculated in terms of the path metrics of the previous iteration as follows:

For Path metric PM_t

$PM_t(p) = \min \{PM_{t-1}(i) + BM_t(i,p), PM_{t-1}(j) + BM_t(j,p)\}$

$PM_t(q) = \min \{PM_{t-1}(j) + BM_t(j,q), PM_{t-1}(i) + BM_t(i,q)\}$

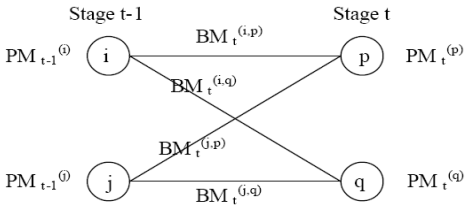

Figure 3: Butterfly structure

3.1 Globally Asynchronous Locally Synchronous (GALS)

In asynchronous design local controller replace the global clock for synchronization of different blocks. In bundle data protocol data and handshakes have separate lines. GALS system is a mixture of synchronous blocks and asynchronous interfaces. It uses the advantages of both synchronous and asynchronous circuits. Each block in GALS is designed as synchronous and they are synchronizes asynchronously. Thus all different blocks interact asynchronously without global clock. There is no any well designed algorithm for GALS, hence very difficult to implement these systems [9]. The problem of clock skew becomes more serious as the technology advances and the frequency increases. As asynchronous systems do not have global clock and thus they are not suffer from the clock skew problem. In GALS system clocks are confined to smaller areas so clock skew is reduced.

IV. Hybrid Registers Exchange Method

Hybrid register exchange method (HREM) for decoding purpose is being used to design VD. Combining the REM and TB techniques is one of the competent solutions to cut the switching activity. In hybrid register exchange method initial state can be first traced through an m cycle, and then transfer the content of initial state to the current state and the next m bits of the register is the m bits of current state itself.

Figure 4 shows example of hybrid register exchange method. Here in the Figure 3 pre-traceback information at t = 4 is 11 for state S1 therefore the content of S1 state register at t = 4 is the data of S3 at t = 2 and the state S1 itself. And at t = 6 the pre-trace-back information of state S2 is 01, therefore the content of S2 state register at t = 6 is the data of S1 at t = 4 and the state S1 itself. This process goes continue, the final state register contains the decoded output. The memory operation is not at every cycle therefore it get reduced by a factor of m, also the shifting of data from one register to another is reduced that is the switching activity will reduce.

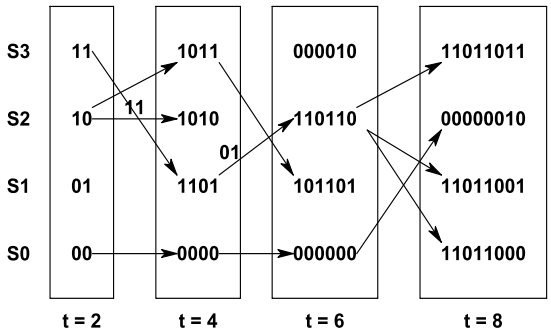

Figure 4: Example of Hybrid Registers Exchange Method

V. Results & Discussion

Viterbi decoder is designed using synchronous and asynchronous register exchange and hybrid register exchange method. The output waveform of the synchronous and asynchronous VD using HREM is shown in figure 6 and figure 7 respectively. VD is designed in VHDL using Xilinx 13.1. A simulation result shows the dynamic power consumption for all four designs at different frequencies.

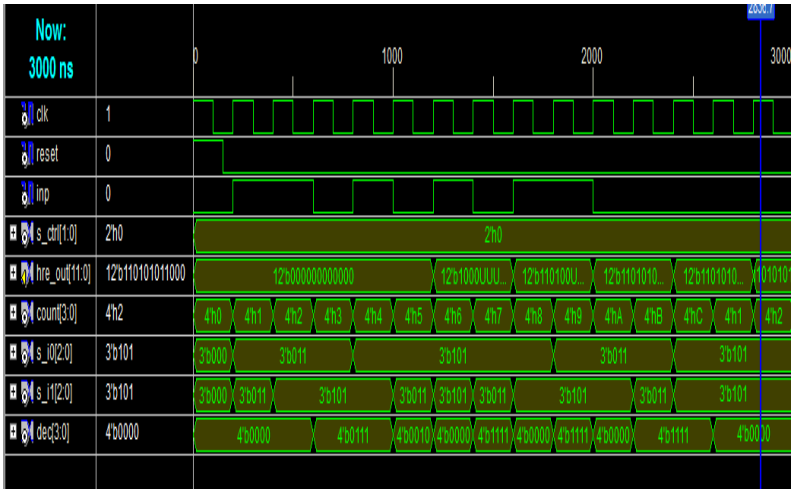

Figure 6: Simulation results of Synchronous Viterbi Decoder Using HREM

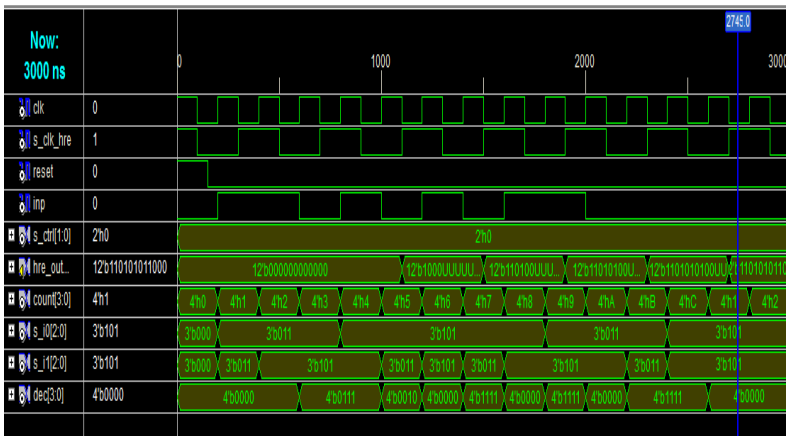

Figure 7: Simulation results of Asynchronous Viterbi Decoder Using HREM

The dynamic power calculated for synchronous and asynchronous design is given in table 1. Asynchronous hybrid register exchange outperforms over synchronous and asynchronous register exchange & synchronous HREM. Both register exchange and hybrid register exchange module have been designed in synchronous and asynchronous technique. Asynchronous Hybrid register exchange method gives the 13.04 % reduction in dynamic power consumed when compared with its synchronous counterpart with much better increase in maximum frequency by 52.71%. With the aid of GALS system power consumption is reduced in both register exchange and hybrid register exchange when compared with their synchronous design.

Table 1: Comparison of Power and maximum frequency between different designs

Clock Frequency	Dynamic Power (mW)			
	Synchronous REM	Asynchronous REM	Synchronous HREM	Asynchronous HREM
5 MHz	0.44	0.36	0.23	0.20
10 MHz	0.77	0.58	0.55	0.38
20 MHz	1.54	1.24	0.84	0.57
50 MHz	4.23	3.86	2.19	1.66
100 MHz	9.24	8.51	4.38	3.34
200 MHz	18.34	17.15	8.94	6.92

Dynamic power mainly depends on the switching activity of the circuit, frequency, load capacitance and supply voltage is given by equation

$$P_{dynamic} = CV\text{^}2f\alpha \quad \text{--- (1)}$$

Where C is load capacitance, V is supply voltage f is clock frequency and α is switching activity. By use of HREM value of 'α' is decreased which helps in reducing the dynamic power of VD.

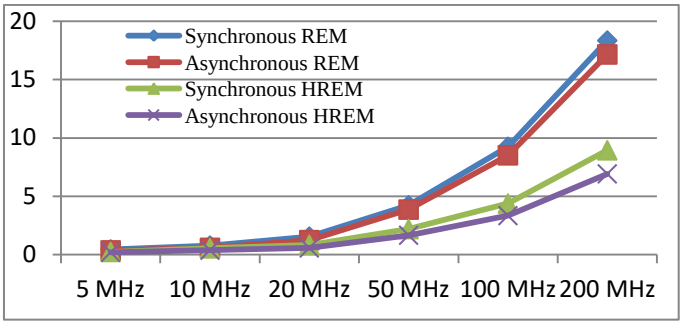

Figure 5: Dynamic Power analysis of different design

Dynamic power analysis of different desin of VD is depicted in figure 5. From equation (1) it shows that dynamic power can be reduced by reducing the supply vltage or load capacitance. It can also be reduce by decrease in clock frequency or switching activity. With the use of HREM switching activity is reduced which helps in reducing the power as compared to REM. GALS system adds the flavour of asynchrony to help in reducing the power decipation. As depicted in table 1 asynchronous HREM gives the lower power as compared to VD designed using synchronous HREM, REM and asynchronous REM.

VI. Conclusions

As we have seen, asynchronous design is a rich area of research, with many different approaches to circuit synthesis. In this paper, we discuss a formal specification of synchronous and asynchronous Viterbi decoder. The decoder design is 4-state, 1/2-rate Viterbi decoder, and the generator polynomials used are the industrial standards (7_8, 5_8). Because of advantage of low switching activity and power consumption asynchronous technique is used to design Viterbi decoder. GALS design is used which is not completely asynchronous but individual synchronous blocks are interface to make system asynchronous. In asynchronous HREM design dynamic power is reduced up-to 13.04% with improvement in system performance when compared with its synchronous counterpart. The complete design is carried out using VHDL in Xilinx ISE 13.1 with family Cyclone IV GX and device used EP4CGX15BF14C6. Power is calculated using Power analysis tool of Quartus II.

References

[1] Mohamed Kawokgy C. André T. Salama, "Low-Power Asynchronous Viterbi Decoder for Wireless Applications", ISLPED? 2004, August 9-11, 2004, Newport Beach, California, USA.
[2] Matheus Trevisan Moreira and Ney Laert Vilar Calazans, "Proposal of an Exploration of Asynchronous Circuits Templates and their Applications", TECHNICAL REPORT SERIES, Number 077, March, 2014, http://www.inf.pucrs.br.
[3] Dr H. Meliani, A. Guellal, "Comparison Between Viterbi Algorithm Soft and Hard Decision Decoding".
[4] Johanna Tuominen, Juha Plosila, "Asynchronous Viterbi Decoder in Action Systems", TUCS Technical Report No 710, September 2005.
[5] S. L. Haridas and Dr. N. K. Choudhari.2010 "A low power Viterbi decoder design with minimum transition hybrid register exchange processing for wireless applications". International journal of VLSI design & Communication Systems (VLSICS) Vol.1, No.4, December 2010.
[6] Scott Hauck, "Asynchronous Design Methodologies: An Overview", Proceedings of the IEEE, Vol. 83, No. 1, pp. 69-93, January, 1995.
[7] B. Javadi, M. Nanderi, H. Pedrams, A. Afzali M. K. Akbari, "An Asynchronous Viterbi Decoder for Low power Applications", PATMOS 2003,LNCS2799, pp 471-480, Springer Verlag Berling Heidelberg 2003.
[8] Mr. G. D. Korde, Dr. S. L. Haridas, "Review of Low Power Asynchronous Viterbi Decoder", Inter-National Conference, ICCCI-2013 at Sri Shakti Institute of Engineering and Technology, Coimbatore, Tamilnadu, January 2013.
[9] Sun-Yen Tan, "A VHDL based design methodology for asynchronous circuits", PhD thesis, 2001.

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